

FIG. 1A



VOLTAGE BETWEEN CONDUCTORS (DC OR AC PEAKS)	MINIMUM SPACING						
	BARE BOARD				ASSEMBLY		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm	0.1 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm
16-30	0.05 mm	0.1 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm
31-50	0.1 mm	0.6 mm	0.6 mm	0.6 mm	0.13 mm	0.13 mm	0.13 mm
51-100	0.1 mm	0.6 mm	0.6 mm	1.5 mm	0.13 mm	0.13 mm	0.13 mm
101-150	0.2 mm	0.6 mm	0.6 mm	3.2 mm	0.13 mm	0.4 mm	0.4 mm
151-170	0.2 mm	1.25 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.4 mm
171-250	0.2 mm	1.25 mm	1.25 mm	6.4 mm	0.4 mm	0.4 mm	0.4 mm
251-300	0.2 mm	1.25 mm	1.25 mm	12.5 mm	0.4 mm	0.4 mm	0.8 mm
301-500	0.25 mm	2.5 mm	2.5 mm	12.5 mm	0.8 mm	0.8 mm	0.8 mm
>500 SEE PARA. 6.3 FOR CALC.	0.0025 mm /VOLT	0.005 mm /VOLT	0.025 mm /VOLT	0.00305 mm /VOLT	0.00305 mm /VOLT	0.00305 mm /VOLT	0.00305 mm /VOLT

FIG. 1B

- B1 - INFORMAL CONDUCTORS
- B2 - EXTERNAL CONDUCTORS, UNCOATED, SEA LEVEL TO 3050 M
- B3 - EXTERNAL CONDUCTORS, WITH PERMANENT POLYMER COATING (ANY ELEVATION)
- A5 - EXTERNAL CONDUCTORS, WITH CONFORMAL COATING OVER ASSEMBLY (ANY ELEVATION)
- A6 - EXTERNAL COMPONENT TERMINATION, UNCOATED
- A7 - EXTERNAL COMPONENT LEAD TERMINATION, WITH CONFORMAL COATING (ANY ELEVATION)



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Attorney Docket: US018102
Title: Single Package Containing Multiple Integrated Circuit Devices
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3/8

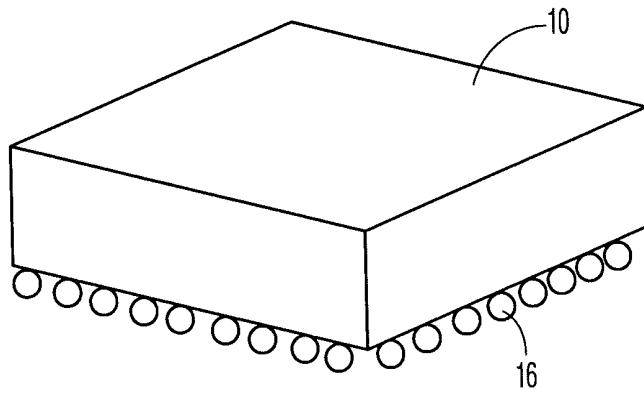


FIG. 2A

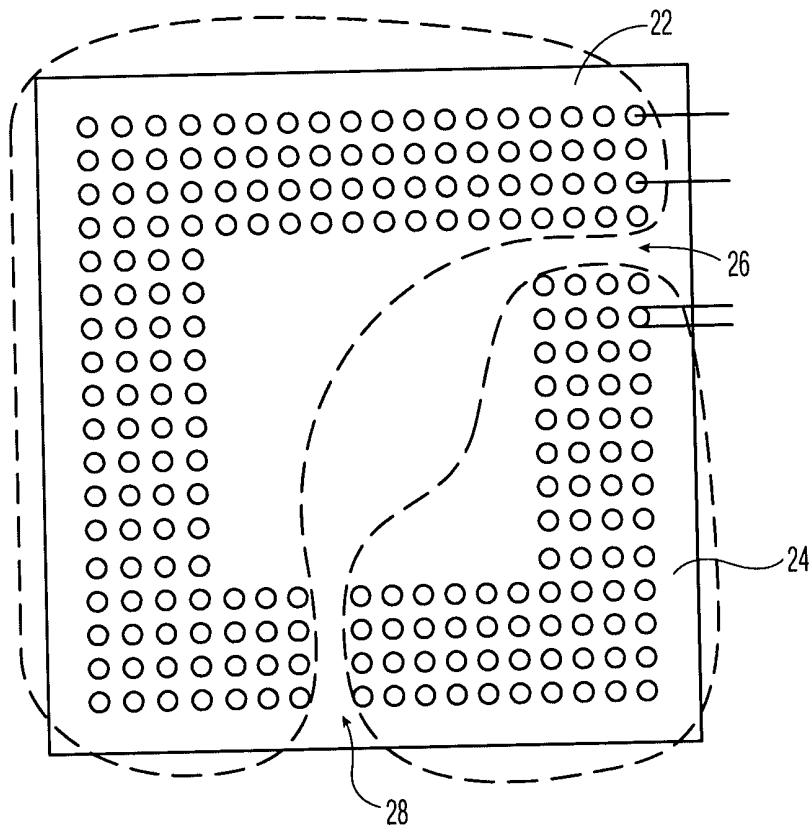


FIG. 2B

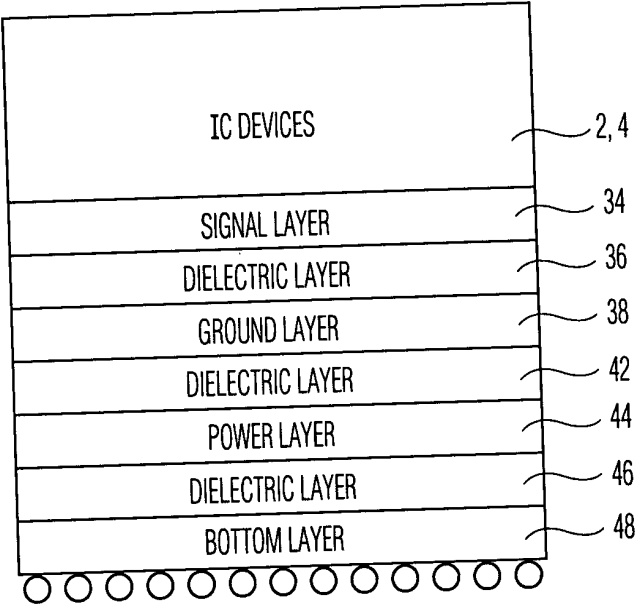


FIG. 3



5/8

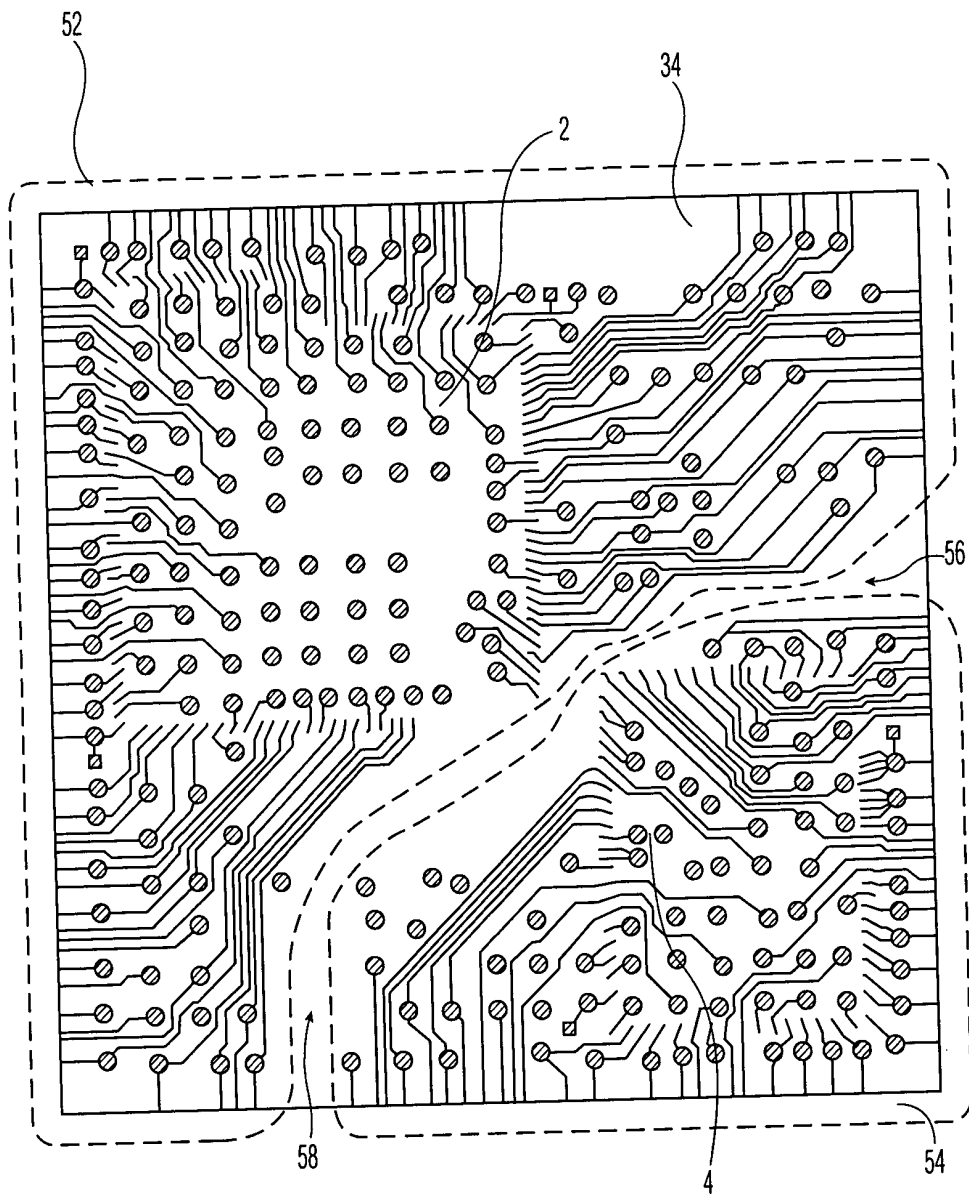


FIG. 4A

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6/8

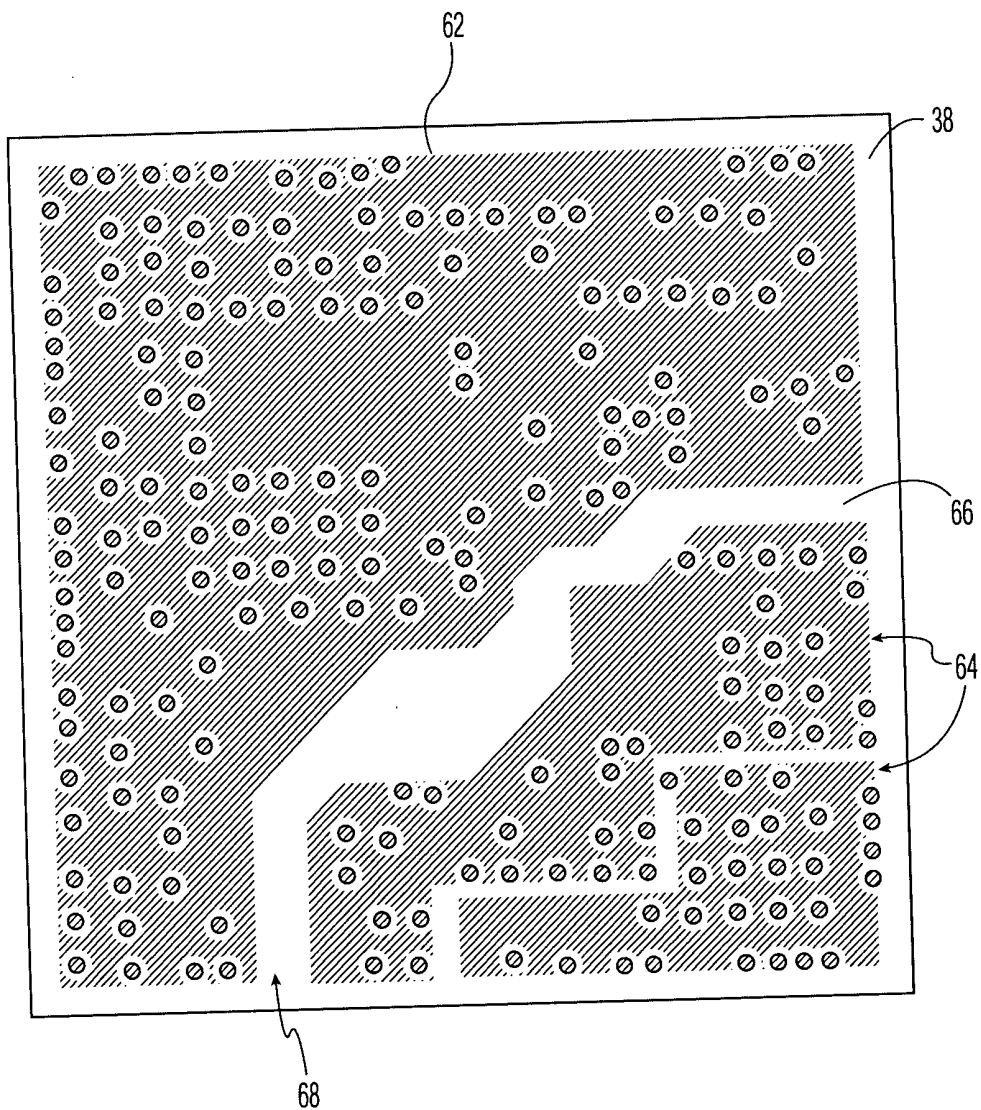


FIG. 4B

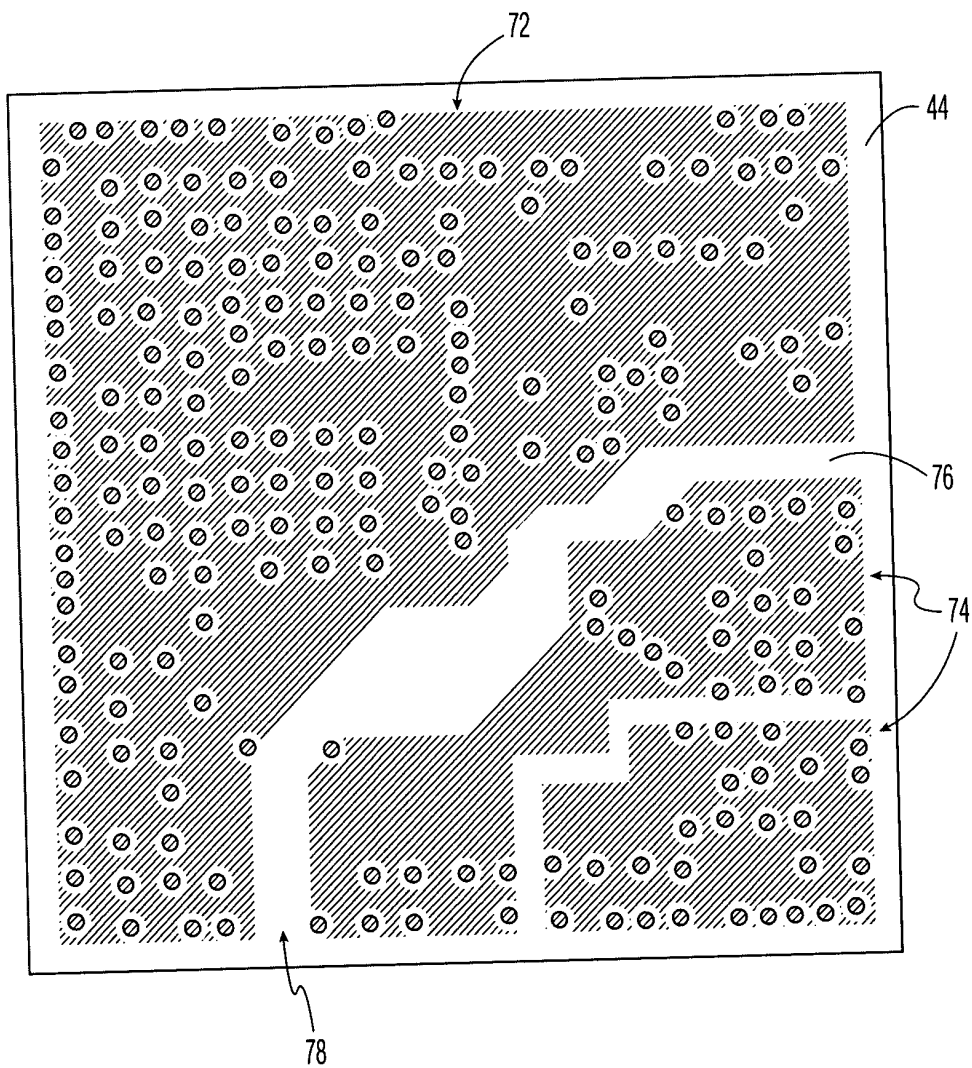


FIG. 4C

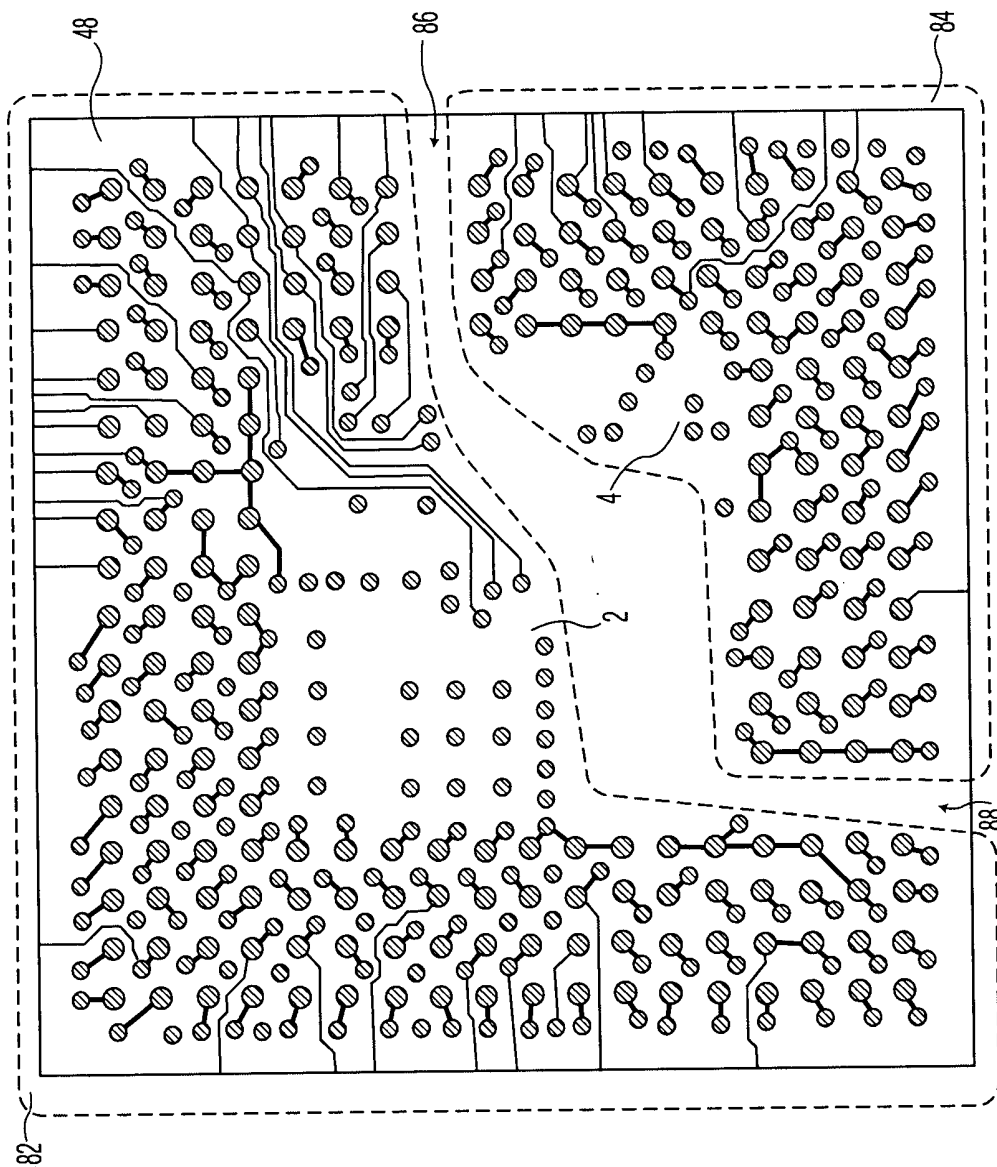


FIG. 4D